



Mirror Technologies

Reflecting Ideas..

- ✓ **100 % OUTPUT AND QUALITY ASSURANCE**
- ✓ **100% PRACTICAL TRAINING ON ALL DOMAINS**

VLSI IEEE PROJECT TITLES LIST

TECHNONLOGY : VLSI

DOMAIN : IEEE TRANSACTIONS ON IMAGEPROCESSING VLSI

S.NO	CODE	TITLES
1	VLSIM01	A NON LINEAR EQUATION BASED CRYPTOSYSTEM FOR IMAGE ENCRYPTION AND DECRYPTION (2012)
2	VLSIM02	A PIPELINE VLSI ARCHITECTURE FOR FAST COMPUTATION OF THE 2-D DISCRETE WAVELET TRANSFORM (2012)
3	VLSIM03	AREA AND POWER EFFICIENT VLSI ARCHITECTURE FOR DCT (2012)
4	VLSIM04	VLSI ARCHITECTURE OF ARITHMETIC CODER USED IN SPIHT (2012)
5	VLSIM05	AN EFFICIENT DENOISING ARCHITECTURE FOR REMOVAL OF IMPULSE NOISE IN IMAGES (2012)
6	VLSIM06	A VLSI ARCHITECTURE AND THE FPGA PROTOTYPE FOR MPEG-4 VIDEO CODEC (2011)
7	VLSIM07	THROUGHPUT EFFICIENT PARALLEL IMPLEMENTATION OF SPIHT ALGORITHM
8	VLSIM08	AN EFFICIENT HARDWARE ARCHITECTURE FOR MULTIMEDIA ENCRYPTION AND AUTHENTICATION USING THE DISCRETE WAVELET TRANSFORM
9	VLSIM09	NOVEL AREA-EFFICIENT FPGA ARCHITECTURES FOR FIR FILTERING WITH SYMMETRIC SIGNAL EXTENSION
10	VLSIM10	FPGA REALIZATION OF LIFTING BASED FORWARD DISCRETE WAVELET TRANSFORM FOR JPEG 2000

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11	VLSIM11	A DETECTION ALGORITHM FOR ZERO-QUANTIZED DCT COEFFICIENTS IN JPEG
12	VLSIM12	NOVEL HARDWARE IMPLEMENTATION OF ADAPTIVE MEDIAN FILTERS
13	VLSIM13	THE REALIZATION OF FFT ALGORITHM BASED ON FPGA CO-PROCESSOR
14	VLSIM14	CONFIGURABLE MULTIRATE FILTER BANKS
15	VLSIM15	AREA EFFICIENT FIR FILTERS FOR HIGH SPEED FPGA IMPLEMENTATION
16	VLSIM16	VLSI IMPLEMENTATION OF HIGH SPEED AND HIGH RESOLUTION FFT ALGORITHM BASED ON RADIX 2 FOR DSP APPLICATION
17	VLSIM17	A VLSI PROGRESSIVE CODING FOR WAVELET-BASED IMAGE COMPRESSION
18	VLSIM18	DESIGN OF INVISIBLE DIGITAL WATERMARKING ALGORITHMS TOWARDS THE DEVELOPMENT OF A SECURE JPEG ENCODER
19	VLSIM19	AN AREA EFFICIENT HIGH PERFORMANCE DCT DISTRIBUTED ARCHITECTURE FOR VIDEO COMPRESSION
20	VLSIM20	A PROCESSOR-IN-MEMORY ARCHITECTURE FOR MULTIMEDIA COMPRESSION
21	VLSIM21	A NOVEL, EFFICIENT ARCHITECTURE FOR THE 2D, LIFTING- BASED DWT WITH FOLDED AND PIPELINED SCHEMES
22	VLSIM22	DESIGN OF A LOSSLESS PARALLEL HIGH-SPEED DATA COMPRESSION SYSTEM
23	VLSIM23	PARALLEL SYNTHESIZABLE IMPLEMENTATION OF 2D DCT IN VHDL

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24	VLSIM24	DESIGN OF HIGH-PERFORMANCE FINITE IMPULSE RESPONSE FILTERS ON FPGAS
25	VLSIM25	DESIGN OF HIGH-PERFORMANCE INFINITE IMPULSE RESPONSE FILTERS ON FPGA
26	VLSIM26	DESIGN OF 8-POINT FFT USING VHDL
27	VLSIM27	IMPROVING AREA EFFICIENCY OF FIR FILTERS IMPLEMENTED USING DISTRIBUTED ARITHMETIC
28	VLSIM28	DESIGN OF HIGH SPEED DECIMATION AND INTERPOLATION FILTER
29	VLSIM29	AN EFFICIENT FPGA IMPLEMENTATION OF A PULSE-SHAPING IIR FILTER
30	VLSIM30	AN FIR NOTCH FILTER FOR ADAPTIVE FILTERING OF A SINUSOIDAL SIGNAL
31	VLSIM31	INVISIBLE IMAGE WATER MARKING TECHNIQUE
32	VLSIM32	DESIGN OF FIR-LOW PASS FILTER USING VHDL/VERILOG

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