Mirror Technologies

Reflecting Ideas..

✓ ***100 % OUTPUT AND QUALITY ASSURANCE***

✓ ***100% PRACTICAL TRAINING ON ALL DOMAINS***

VLSI IEEE PROJECT TITLES LIST

TECHNONLOGY : VLSI

DOMAIN : IEEE TRANSACTIONS ON LOWPOWER VLSI

S.NO	CODE	TITLES
1	VLSIL01	IMPACT OF RANDOM DOPANT FLUCTUATIONS ON THE TIMING CHARATERISTICS OF FLIP-FLOPS
2	VLSIL02	LOW POWER DUAL EDGE TRIGGERED FLIP-FLOP
3	VLSIL03	IMPLEMENTATION OF FULL ADDER CELLS USING NP-CMOS AND MULTI-OUTPUT LOGIC STYLES IN 90NM TECHNOLOGY
4	VLSIL04	DESIGN OF LOW POWER HIGH SPEED VLSI ADDER SUBSYSTEM
5	VLSIL05	DELAY BASED DUAL RAIL PRECHARGE LOGIC
6	VLSIL06	AN ENERGY EFFICIENT SECURE LOGIC TO PROVIDE RESISTANCE AGAINST DIFFERENTIAL POWER ANALYSIS ATTACKS
7	VLSIL07	POWER-EFFICIENT EXPLICIT-PULSED DUAL-EDGE TRIGGERED SENDE-AMPLIFIER FLIP-FLOPS
8	VLSIL08	PERFORMANCE ANALYSIS OF POWER GATING DESIGNS IN LOW POWER VLSI CIRCUITS
9	VLSIL09	LOW POWER VLSI CIRCUIT IMPLEMENTATION USING MIXED STATIC CMOS AND DOMINO LOGIC WITH DELAY ELEMENTS
10	VLSIL10	ENERGY RECOVERY PERFORMANCE OF QUASI-ADIABATIC CIRCUITS USING LOWER TECHNOLOGY NODES

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11	VLSIL11	POWER COMPARISON OF CMOS AND ADIABATIC FULL ADDER CIRCUITS
12	VLSIL12	DESIGN OF SEQUENTIAL ELEMENTS FOR LOW POWER CLOCKING SYSTEM
13	VLSIL13	LOW-VOLTAGE AND LOW-POWER CONSUMPTION 0.35UM CMOS VOLTAGE-MODE DEFUZZIFIER
14	VLSIL14	ENERGY EFFICIENT ADIABATIC LOGIC FOR LOW POWER VLSI APPLICATIONS
15	VLSIL15	BZ-FAD: A LOW-POWER LOW-AREA MULTIPLIER BASED ON SHIFT-AND-ADD ARCHITECTURE
16	VLSIL16	LOW-POWER AES DESIGN USING PARALLEL ARCHITECTURE
17	VLSIL17	LOW POWER FFT DESIGN FOR WIRELESS COMMUNICATION SYSTEMS
18	VLSIL18	ESTIMATING POWER CONSUMPTION FOR FIR FILTER IMPLEMENTATION ON FPGA
19	VLSIL19	A BIST TPG FOR LOW POWER DISSIPATION AND HIGH FAULT COVERAGE
20	VLSIL20	LOW POWER STATE-PARALLEL RELAXED ADAPTIVE VITERBI DECODER DESIGN AND IMPLEMENTATION
21	VLSIL21	FPGA IMPLEMENTATION OF LOW POWER PARALLEL MULTIPLIER
22	VLSIL22	LOW POWER FPGA-BASED IMPLEMENTATION OF DECIMATING FILTERS FOR MULTISTANDARD RECEIVER
23	VLSIL23	AN EFFICIENT SPURIOUS POWER SUPPRESSION TECHNIQUE (SPST) AND ITS APPLICATIONS ON MPEG-4 AVCLH.264 TRANSFORM CODING DESIGN

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24	VLSIL24	A LOW-POWER VITERBI DECODER DESIGN FOR WIRELESS COMMUNICATIONS APPLICATIONS