



# Mirror Technologies

*Reflecting Ideas..*

- ✓ **100 % OUTPUT AND QUALITY ASSURANCE**
- ✓ **100% PRACTICAL TRAINING ON ALL DOMAINS**

## **VLSI IEEE PROJECT TITLES LIST**

### **TECHNONLOGY: VLSI**

<b>S.NO</b>	<b>TITLES</b>
1	RELAXED FAULT-TOLERANT HARDWARE IMPLEMENTATION OF NEURAL NETWORKS IN THE PRESENCE OF MULTIPLE TRANSIENT ERRORS (2012)
2	USING MAGNETIC RAM TO BUILD LOW-POWER AND SOFT ERROR-RESILIENT L1 CACHE (2010)
3	ANALYSIS AND COMPENSATION OF THE EFFECTS OF ANALOG VLSI ARITHMETIC ON THE LMS ALGORITHM (2011)
4	VARIABLE LATENCY GOLDSCHMIDT ALGORITHM BASED ON A NEW ROUNDING METHOD AND A REMAINDER ESTIMATE (2011)
5	A GOLDSCHMIDT DIVISION METHOD WITH FASTER THAN QUADRATIC CONVERGENCE (2011)
6	RISC BASED ARCHITECTURE FOR COMPUTER HARDWARE INTRODUCTION (2011)
7	A NEW COMPACT SD2 POSITIVE INTEGER TRIANGULAR ARRAY DIVISION CIRCUIT (2011)
8	BUILDING AN AMBA AHB COMPLIANT MEMORY CONTROLLER (2011)
9	USING QUANTUM CRYPTOGRAPHY FOR SECURING WIRELESS LAN NETWORKS (2011)
10	HAMMING DISTANCE BASED REORDERING AND COLUMNWISE BIT STUFFING WITH DIFFERENCE VECTOR:A BETTER SCHEME FOR TEST DATA COMPRESSION WITH RUN LENGTH BASED CODES (2010)
11	OPTIMIZATION CONCEPTS FOR SELF-HEALING ASYNCHRONOUS CIRCUITS (2011)

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12	A TIME-AREA- POWER EFFICIENT MULTIPLIER AND SQUARE ARCHITECTURE BASED ON ANCIENT INDIAN VEDIC MATHEMATICS (2011)
13	DESIGN AND IMPLEMENTATION OF AN OFDM SYSTEM FOR VEHICULAR COMMUNICATIONS WITH FPGA TECHNOLOGIES
14	A NEW VLSI ARCHITECTURE OF PARALLEL MULTIPLIER-ACCUMULATOR BASED ON RADIX-2 MODIFIED BOOTH ALGORITHM
15	AREA EFFICIENT VLSI ARCHITECTURE OF LMS ADAPTIVE EQUALIZER FOR OFDM
16	IMPLEMENTATION OF LOW COST BIST CIRCUIT FOR PUBLIC KEY CRYPTOCORES
17	COMPACT FPGA BASED ARCHITECTURE FOR ELLIPTIC CURVE CRYPTOGRAPHY OVER PRIME FIELDS
18	INITIALIZATION-BASED TEST PATTERN GENERATION FOR ASYNCHRONOUS CIRCUITS
19	AN FPGA BASED CONTROL ALGORITHM FOR CASCADED MULTILEVEL INVERTERS
20	STANDBY LEAKAGE POWER REDUCTION IN CMOS NANO VQJ DEVICE
21	A MIXED STYLE MULTIPLIER ARCHITECTURE FOR LOW DYNAMIC AND LEAKAGE POWER DISSIPATION
22	SELF-TEST TECHNIQUES FOR CRYPTO-DEVICES
23	DYNAMIC BIT-WIDTH ADAPTATION IN DCT: AN APPROACH TO TRADE OFF IMAGE QUALITY AND COMPUTATION ENERGY
24	POWER ESTIMATION OF EMBEDDED MULTIPLIER BLOCKS IN FPGAS

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25	RECURSIVE PSEUDO-EXHAUSTIVE TWO-PATTERN GENERATION
26	NEW ARCHITECTURAL DESIGN OF CA-BASED CODEC
27	AN EFFICIENT MULTIMODE MULTIPLIER SUPPORTING AES AND FUNDAMENTAL OPERATIONS OF PUBLIC-KEY CRYPTOSYSTEMS
28	IMPROVING FPGA PERFORMANCE FOR CARRY-SAVE ARITHMETIC
29	COST EFFICIENT FEQ IMPLEMENTATION FOR IEEE 802.16A OFDM TRANSCEIVER

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